IDEC Chip Design Contest

A Digitalized Chaotic Oscillator Probabilistic Bit For Static Annealing Ising Machine

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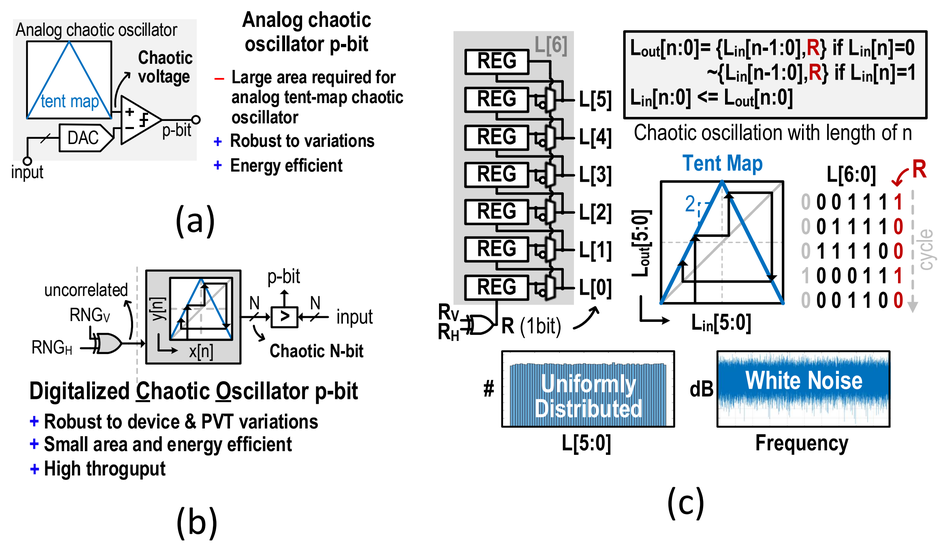
Introduction

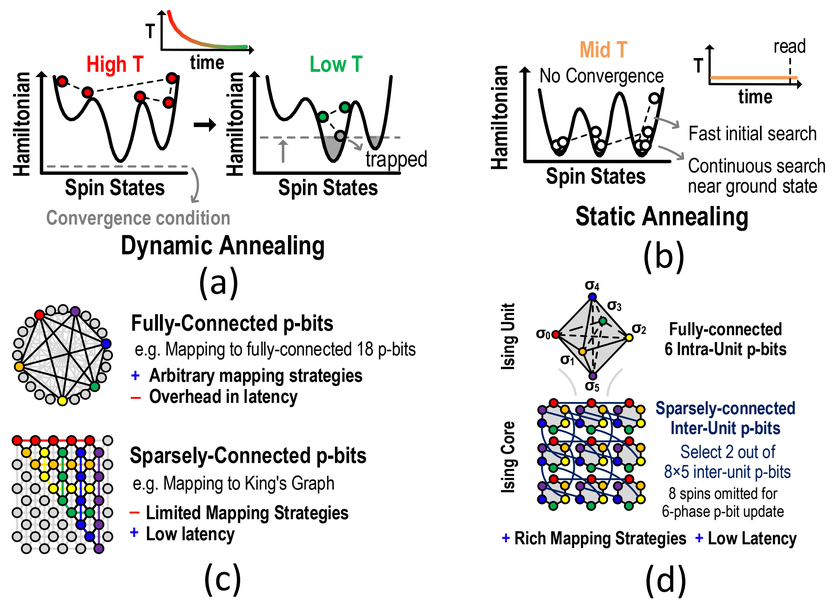
This work presents a digital tent-map chaotic oscillator (DCO)-based probabilistic bit (p-bit) architecture for compute-in-memory probabilistic computing applications. Unlike conventional p-bits, the DCO-based p-bit take both advantage of high throughput and robustness of pseudo-random number generator (PRNG)-based p-bits and small area consumption of analog domain p-bits. The DCO achieves high energy efficiency of 0.041 pJ/bit. We apply this noise generator to static annealing, a schedule that maintains fixed temperature during operation, and demonstrate its effectiveness on the Max-Cut problem. Compared to conventional thermal annealing approaches that rely on gradually changing temperatures, the static annealing scheme converges faster and achieves lower final Hamiltonian values in our experiments. Our findings highlight that static annealing is not only feasible but advantageous in solving complex problems with compute-in-memory hardware.

Digitalized Chaotic Oscillator



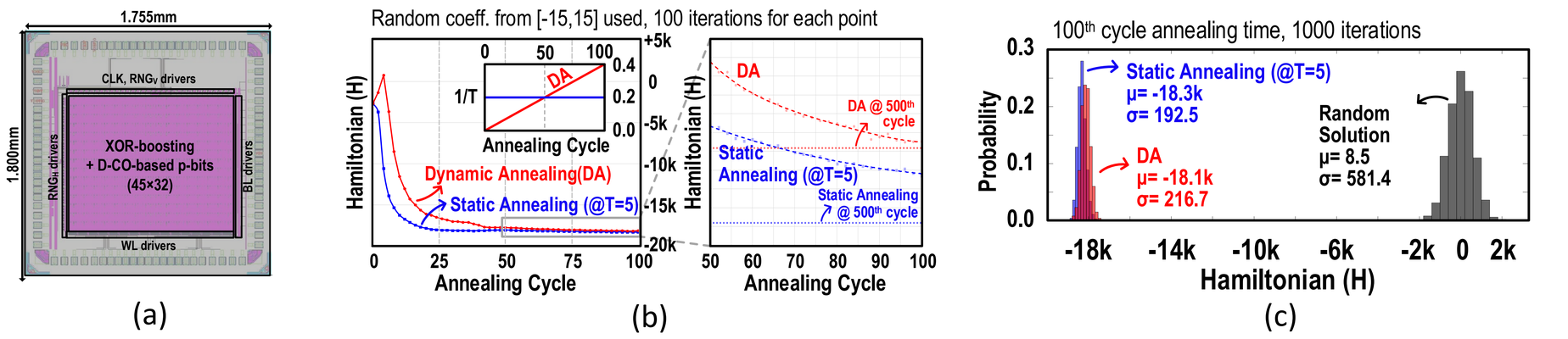
- (a) shows the block diagram of analog tent-map chaotic oscillator (ACO) [1]. It is robust to PVT variation, however, consumes large area.
- (b) shows the proposed digitalized tent-map chaotic oscillator (DCO).
- (c) shows the schematic and operation of the proposed DCO. The output of DCO shows uniformly distributed, white noise characteristics.

Static Annealing and Hybrid Connection



- (a) shows conventional annealing schedule, dynamic annealing [2]–[3].
- (b) shows the proposed static annealing schedule. Static annealing shows fast initial search and continuous search without local trap.
- (c) shows conventional connections of p-bits [1], [4], whereas (d) shows proposed hybrid connection. Both rich mapping strategies and low latency can be achieved.

Measurement and Conclusion



- (a) shows a chip layout. The Ising machine is implemented in a 28-nm CMOS process. A single DCO occupies 30.2 μm^2
- (b) shows the transient Hamiltonian using dynamic annealing and static annealing.
- (c) shows the histogram of Hamiltonian at the 100th cycle point
- By replacing the analog chaotic oscillator with a fully digital circuit, the proposed DCO achieves high PVT robustness, compact area, and high energy efficiency of 0.041 pJ/bit, which is over 100 times lower than prior analog implementations. Simulated results show that static annealing achieves faster and more stable convergence compared to dynamic annealing, attaining significantly lower average Hamiltonian values.

Acknowledgement

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[1] W. Lee et al., *Sci. Rep.*, vol. 15, no. 8018, Mar. 2025.
[2] N. A. Aadit et al., *Nat. Elec.*, vol. 5, no. 7, pp. 460-468, June 2022.
[3] K. Yamamoto et al., *IEEE JSSC*, vol. 56, pp. 165-178, Jan. 2021.
[4] H. Jung et al., *Sci. Rep.* vol. 13, no. 16186, Sep. 2023.